

[illegible]

A cross-sectional view of a semiconductor device. It shows a substrate 11 with a top layer 12. A trench 13 is formed in the top layer 12, extending into the substrate 11. The trench 13 has a bottom surface 15 and side walls 16. A layer 21 is deposited on the bottom surface 15 and side walls 16. A layer 22 is deposited on top of layer 21. A layer 23 is deposited on top of layer 22. A layer 24 is deposited on top of layer 23. An arrow points to the bottom surface 15 of the trench 13.

This diagram shows a cross-sectional view of a substrate 11. A conductive layer 12 is formed on the top surface of the substrate 11. A conductive paste 13 is applied to the top surface of the conductive layer 12. A portion of the conductive paste 13 is shown in a hatched pattern, labeled 25. A label 21 points to the conductive layer 12.

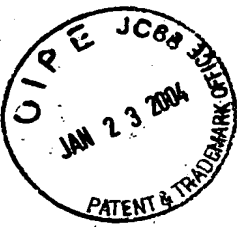


FIG. 7

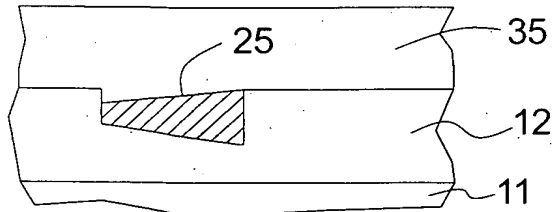


FIG. 8

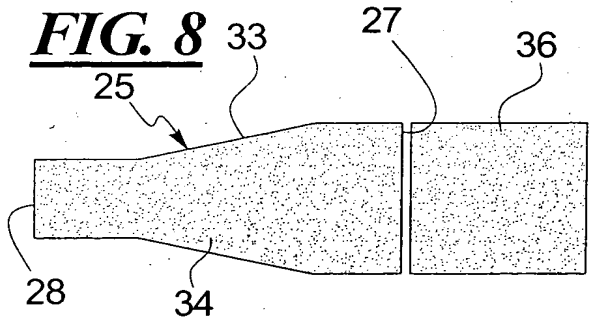


FIG. 9

COUPLING
LOSS (dB)

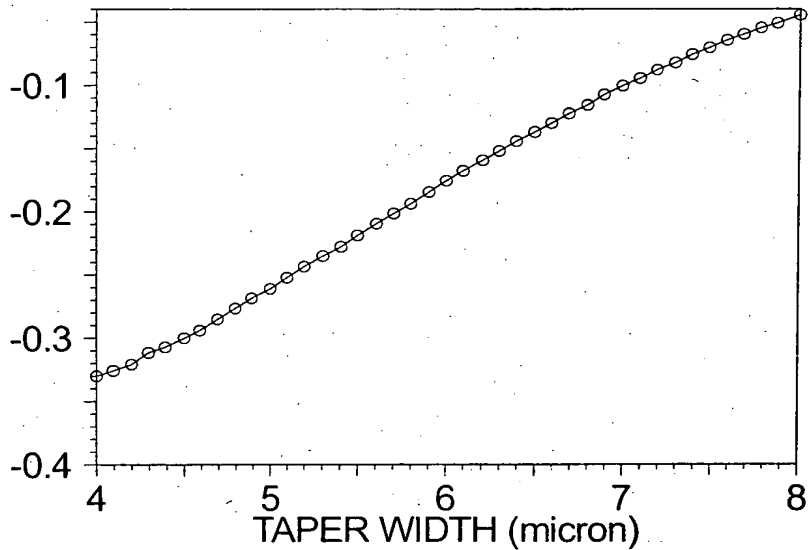


FIG. 10

COUPLING
LOSS (dB)

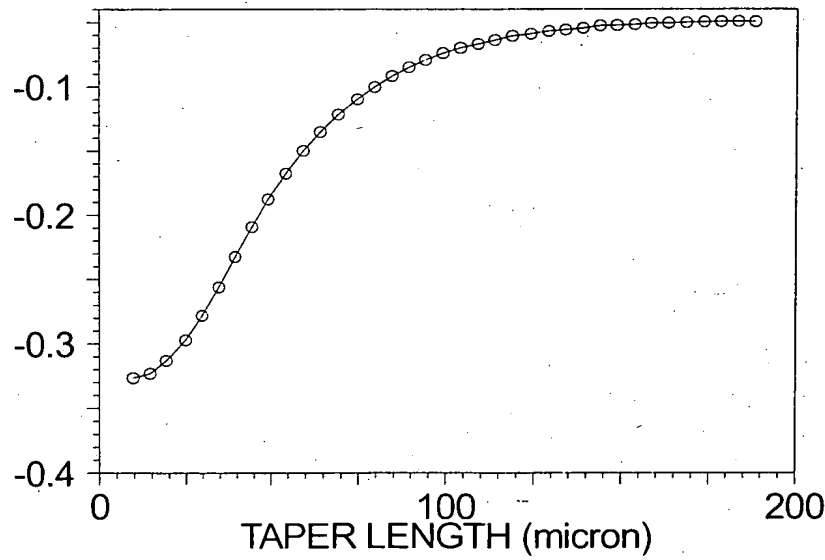
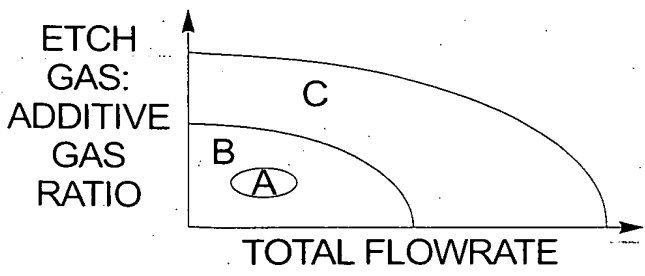


FIG. 11



ETCH RATE OF SMALL FEATURE:
ETCH RATE OF LARGE FEATURE
A \approx 1-2 (REVERSE RIE LAG)
B \approx 1 (NO RIE LAG)
C \approx 0.5 (RIE LAG)